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09/886,081	06/18/2001	Igor Anatoly Gorin	033116-002	5913

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EXAMINER	
STEVENS, THOMAS H	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,081	GORIN ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/31/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 were examined.

Response to Applicant's Arguments

35 USC § 112

2. Applicant's are thanked for addressing this issue. Rejections are withdrawn based applicant's amendment.

35 USC § 103

3. Applicant's are thanked for addressing this issue. Applicants claim Nakaie, doesn't teach or suggest the function or event of a charged capacitor when if fact Nakaie's abstract states: *"...at the integrated circuit for connection to the grounding conductor in order to release electric charge from the integrated circuit to the grounding conductor...* coupled with the following excerpt: *"Because of the smaller inductance L, furthermore, the CMD simulators of this invention can freely make any desired waveform by adding appropriate capacitance* (column 3, lines 14-16).

Since Nakaie is teaching simulation discharge specifically discharged current with appropriate capacitance. One of ordinary skill in the art would deduce that capacitors, by nature, charge and discharge; so the fact Nakaie doesn't state verbatim a "charged capacitor" is immaterial in light of the art taught. Rejection stands.

Final Rejection

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 7-23 are rejected under 35 U.S.C. 103 (a) as unpatentable by the Electronic Industries Association (EIA) JESD22-C101 Test Method (1995), in view of Nakaie et al., (U.S. Patent 5,740,007 (1998)). The EIA standard teaches procedures for field-induced charged device model test method for electrostatic discharge to withstand thresholds of microelectronic components; but doesn't teach an example. Nakaie et al teaches simulation of a charged device model (CDM), which simulates rapid discharges of electricity to check for static-electricity-induced or other damage to integrated circuits

(column 1, lines 1-4). At the time the invention, it would have been obvious to one of ordinary skill in the art to use Nakaie et al. to modify (EIA) to apply the standard to actual practice.

Claim 1. In a CDM simulator for providing a rapid discharge of an electrical current transient to test an electrical device under test, a test circuit comprising (EIA: pg. 1, section 5 with figure 1): an electrically conductive material having a dielectric layer coextensively disposed thereon, said layer being adapted to receive said device when said device is under test (EIA: pg. 1, section 5 with figure 1); a charge capacitor (Nakaie: column 1, lines 38-40); a normally open discharge switch (Nakaie: column 1, lines 46-50) electrically coupled in series between said electrically conductive material and said charge capacitor (Nakaie: column 1, lines 38-40) defining a first node between said charge capacitor and said discharge switch, said first node at least intermittently having a power source resistively connected thereto to store a charge on said charge capacitor; and a resistor adapted to be electrically connected in series between (Nakaie: column 1, lines 38-40) said charge capacitor and said device when said device is under test defining a second node between said resistor and said charge capacitor, said second node being normally grounded (Nakaie: column 1, lines 58-65), whereby closing of said discharge switch subsequent to said charge being stored on said charge capacitor causes said current transient to be discharged through said device under test.

Claim 2. A test circuit as set forth in Claim 1(EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65) wherein said discharge switch is a wet relay switch.

Claim 3. A test circuit as set forth in Claim 1 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65) wherein said discharge switch is a mercury switch (Nakaie: column 2, lines 9-11).

Claim 4. A test circuit as set forth in Claim 1 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65) further comprising a connection wire to be coupled electrically intermediate said resistor (Nakaie: column 1, lines 14-15) and said device under test.

Claim 5. A test circuit as set forth in Claim 4 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65) wherein said connection wire has a predetermined inductance (Nakaie: column 1, lines 14-15) per unit length.

Claim 7. A test circuit as set forth in Claim 1 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65) further comprising a decoupling resistor electrically connected to said first node (Nakaie: column 1, lines 14-15 with EIA: figure 1), said power source being at least intermittently connected to said resistor.

9. Claims 6, 8-23 are rejected under 35 U.S.C. 103 (a) as unpatentable by the Electronic Industries Association (EIA) JESD22-C101 Test Method (1995), in view of Nakaie et al., (U.S. Patent 5,740,007 (1998)) and in further view of Gieser (U. S. Patent 6,512,362 (2003)). The EIA standard teaches procedures for field-induced charged device model test method for electrostatic discharge to withstand thresholds of microelectronic components; but doesn't teach an examples. Nakaie et al teaches simulation of a charged device model (CDM), which simulates rapid discharges of electricity to check for static-electricity-induced or other damage to integrated circuits (column 1, lines 1-4), while Gieser teaches a method and a device wherein a high current pulse can be injected via a terminal into the device under test, where a substrate together with the reference electrode disposed on the actual circuit and determining the loading parameters, which a capacitor has a dielectric (abstract). At the time the invention, it would have been obvious to one of ordinary skill in the art to use Nakaie et al. to modify (EIA) to apply the standard to actual practice.

Claim 6. A test circuit as set forth in Claim 1(EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65) wherein said electrically conductive material is a charge plate having a first surface, said (Gieser: column 5, lines 29-33) dielectric material being disposed on said first surface.

Claim 8. A CDM simulator for providing a rapid discharge of an electrical current transient to a device under test comprising (EIA: pg. 1, section 5 with figure 1; Nakaie:

column 1, lines 38-40, lines 58-65): an electrically conductive material having a dielectric layer coextensively disposed thereon, said layer being adapted to receive said device when said device is under test (Gieser: column 5, lines 29-33 with EIA: figure 1); a charge capacitor (Nakaie: column 1, lines 38-40); a normally open discharge switch electrically coupled in series between said electrically conductive material and said charge capacitor defining a first node between said charge capacitor and said discharge switch (Gieser: column 5, lines 29-33 with EIA: figure 1); a power source resistively connected to said first node to store a charge on said charge capacitor (EIA: PG. 1, section 5.2 with figure 1); and a resistor at least intermittently: electrically connected in series between said charge capacitor and said device when said device is under test defining a second node between said resistor and said charge capacitor, said second node being normally grounded, whereby closing of said discharge switch subsequent to said charge being stored on said charge capacitor causes said current transient to be discharged through said device under test (EIA: PG. 1, section 5.2 with figure 1).

Claim 9. A CDM simulator as set forth in Claim 8 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65; Gieser: column 5, lines 29-33 with EIA: figure 1) wherein said discharge switch is a wet relay switch.

Claim 10. A CDM simulator as set forth in Claim 8 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65; Gieser: column 5, lines 29-33 with EIA:

figure 1) wherein said discharge switch is a mercury switch (Nakaie: column 2, lines 9-11).

Claim 11. A CDM simulator as set forth in Claim 8 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65; Gieser: column 5, lines 29-33 with EIA: figure 1) further comprising a connection wire (Nakaie: column 1, lines 21-25) to be coupled electrically intermediate said resistor (Nakaie: column 1, line 15) and said device under test.

Claim 12. A CDM simulator as set forth in Claim 11(EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65; Gieser: column 5, lines 29-33 with EIA: figure 1) wherein said connection wire (Nakaie: column 1, lines 21-25) has a predetermined inductance (Nakaie: column 1, lines 14-15) per unit length.

Claim 13. A CDM simulator as set forth in Claim 8 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65; Gieser: column 5, lines 29-33 with EIA: figure 1) wherein said electrically conductive material is a charge plate having a first surface, said dielectric material being disposed on said first surface.

Claim 14. A CDM simulator as set forth in Claim 8 (EIA: pg. 1, section 5 with figure 1; Nakaie: column 1, lines 38-40, lines 58-65; Gieser: column 5, lines 29-33 with EIA:

figure 1) further comprising a decoupling resistor electrically (Nakaie: column 1, lines 14-15 with EIA: figure 1) connected between said power source and said first node.

Claim 15. A method for providing a rapid discharge of an electrical current transient to test in situ an electrical device comprising (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15): spacing proximally said device from an electrically conductive material (Gieser: column 1, lines 49-52; and EIA: figure 1); connecting resistively said device to ground potential (EIA: pg. 1, section 5, with figure 1); charging a charge capacitor to store and electrical charge thereon; and injecting said charge into said electrically conductive material whereby said current transient is discharged through said device (Gieser: column 1, lines 12-15).

Claim 16. A method as set forth in Claim 15 (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15) wherein said spacing includes placing a dielectric material intermediate said electrically conductive material and said device (Gieser: column 5, lines 29-35).

Claim 17. A method as set forth in Claim 15 (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15; column 5, lines 29-35) wherein said injecting includes: (Nakaie: column 1, lines 46-50. Note: the capacitor has to charge to discharge); switching said charge to electrically conductive material (EIA: pg. 1, section 5 with figure 1).

Claim 18. A method as set forth in Claim 15(EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15; column 5, lines 29-35) further comprising varying the inductance (Nakaie: column 2, lines 55-57) of a discharge path of said current transient.

Claim 19. A method as set forth in Claim 18 (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15; column 5, lines 29-35) wherein said varying includes electrically connecting variable lengths of a connection wire having a predetermined inductance per unit length (Nakaie: column 2, lines 55-57) in series between said device and ground potential (EIA: pg. 1, section 5 with figure 1; and Gieser: column 1, lines 58-67).

Claim 20. A method for providing a rapid discharge of an electrical current transient to test in situ an electrical device comprising (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15): placing a layer of a dielectric material on a first surface of a discharge plate of an electrically conductive material, said device being placed on said layer (Gieser: column 5, lines 27-35 with figure 1); connecting a resistor in series between said device and ground potential; connecting a normally open discharge switch and a charge capacitor in series between said resistor and said discharge plate wherein a first node is defined between said discharge switch and said discharge capacitor and a second node is defined between said resistor and discharge capacitor, said second node being coupled to

ground potential; and storing a charge on said charge capacitor, whereby closing of said discharge switch injects said charge into said electrically conductive material whereby said current transient is discharged through said device (EIA: pg. 1, section 5 with figure 1; and Gieser: column 1, lines 58-67).

Claim 21. A method as set forth in Claim 20 (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15) wherein said storing includes connecting a power source through a decoupling resistor to said first node when said discharge switch is open (EIA: pg. 1, section 5 with figure 1).

Claim 22. A method as set forth in Claim 20 (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15) further comprising varying the inductance of a discharge (Nakaie: column 2, lines 55-57 with column 1, lines 58-67) path of said current transient.

Claim 23. A method as set forth in Claim 22 (EIA: pg. 1, section 2; Nakaie: column1 and 2, lines 1-20 and lines 14-15, respectively; and Gieser: column 1, lines 12-15) wherein said varying includes electrically connecting variable lengths of a connection wire having a predetermined inductance (Nakaie: column 1, lines 10-20; column 2, lines 56-57) per unit length in series between said device and said resistor.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

March 23, 2005

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER